REMARKS

Claims 4 and 8-12 are pending in the application and stand rejected.

Rejection under 35 U.S.C §102

Claims 4 and 8-12 stand rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 5,252,957 to Itakura. Applicants have reviewed the reference with care, paying particular attention to the passages cited, and are compelled to respectfully disagree with the Examiner's characterization of this reference. More specifically, Applicants submit that Itakura does not in fact teach, disclose or suggest the claimed inverter having an input terminal coupled to a control electrode of a first TFT and an output terminal coupled to a gate terminal of a second TFT, wherein the first and second TFTs are coupled together.

Referring particularly to Fig. 1 of Itakura, a liquid crystal display apparatus driving circuit comprises a plurality of inverters INV respectively coupled to nodes (A)-(E). For the left-most circuit set, a control electrode (gate terminal) of a transistor MS is coupled to an input terminal of an inverter INV which is coupled to a node A, while a control electrode (gate terminal) of a transistor MC is coupled to an output terminal of an inverter INV which is coupled to a node B. The drain and source of the transistor MC are coupled together to one terminal of the transistor MS. As clearly shown in Fig. 1, the input terminal coupled to the transistor MS and the output terminal coupled to the transistor MC are from two different inverters - in other words, the transistors MS and MC are coupled together and are also coupled to *different* inverters.

Contrary to Itakura as discussed above, the circuit recited in claim 4 includes an inverter has an input terminal and an output terminal wherein a control electrode of a first TFT is coupled to the input terminal of the inverter and a gate terminal of a second TFT is coupled to the output terminal of the inverter. Both the drain and source terminals of the second TFT are coupled to a second electrode of the first TFT. Thus, the first and second TFTs that are coupled together are

coupled to the *same* inverter. At least for this reason, Applicants submit that Itakura therefore clearly does not anticipate the circuit of claim 4.

Applicants further submit that claim 8 is also novel over Itakura for the same reasons as set forth above with respect to claim 4.

With respect to claim 9, Applicants submit that Itakura does not in fact teach, disclose or suggest the claimed inverter having an input terminal coupled to a control electrode of a first TFT and an output terminal coupled to a capacitor, wherein the capacitor is coupled between the output terminal and a second electrode of the first TFT.

In particular, and referring once again to Fig. 1 of Itakura, the drain and source of the transistor MC are coupled together to one terminal of the transistor MS and thus the transistor MC serves as a capacitor coupled between the transistor MS and the inverter coupled to node B. According to Fig. 1 and as previously noted, the input terminal coupled to the transistor MS and the output terminal coupled to transistor MC (that is, the capacitor) belong to two *different* inverters, and thus the transistor MS and the capacitor/transistor MC that are coupled together are in turn coupled to different inverters.

On the other hand, present claim 9 recites an inverter having an input terminal and an output terminal wherein a control electrode of a first TFT is coupled to the input terminal of the inverter and a capacitor is coupled between a second electrode of the first TFT and the output terminal of the inverter. Thus, the first TFT and the capacitor are coupled together and are also coupled to the *same* inverter, in direct contrast to the circuit of Itakura. At least for this reason, Applicants submit that Itakura therefore clearly also does not anticipate the circuit of claim 9.

Applicants further submit that claim 11 is also novel over Itakura for the same reasons as set forth above with respect to claim 9.

Finally, Applicants note that claims 10 and 12 depend from claims 9 and 11, respectively, and therefore submit that claims 10 and 12 are also allowable over Itakura at least by virtue of their dependencies.

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Regarding the prior art made of record by the Examiner but not relied upon, Applicants believe that this art does not render the pending claims unpatentable.

In view of the above, Applicants submit that the application is now in condition for allowance and respectfully urge the Examiner to pass this case to issue.

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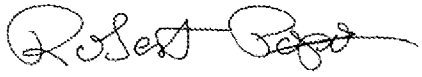
The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account no. 12-0415. In particular, if this response is not timely filed, the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136(a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

I hereby certify that this document is being transmitted to the Patent and Trademark Office via electronic filing.

February 15, 2008
(Date of Transmission)

Respectfully submitted,



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